Provable Security

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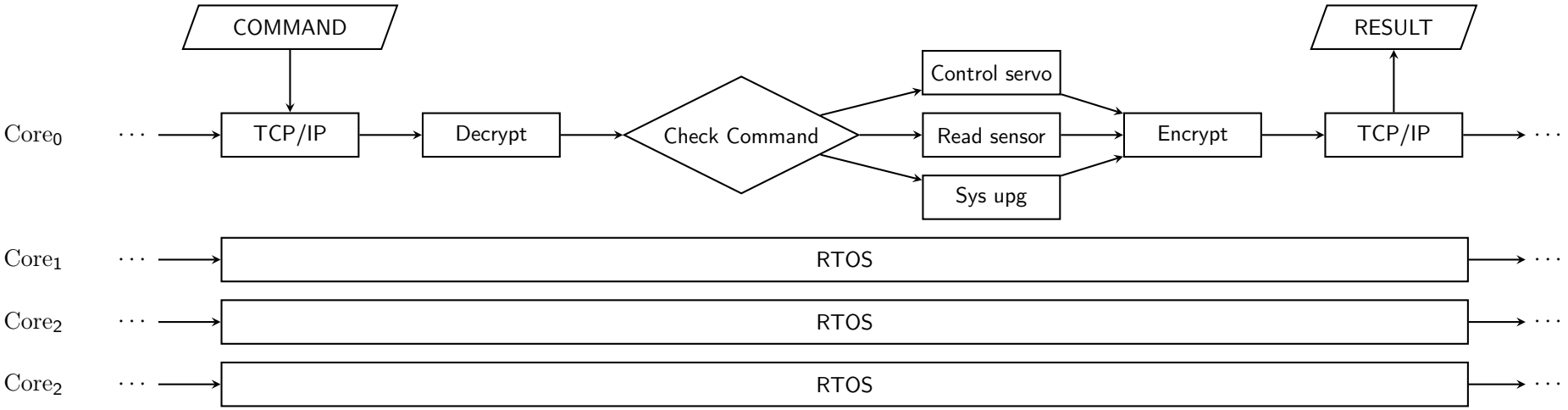
Outline

1. Example Application & Proof-of-Concept
2. Simply Secure Separation Kernel (S3K)
3. S3K Process Scheduling
4. Multicore HolBA & Kernel Verification
5. Research plan

Example Application & Proof-of-Concept

Application



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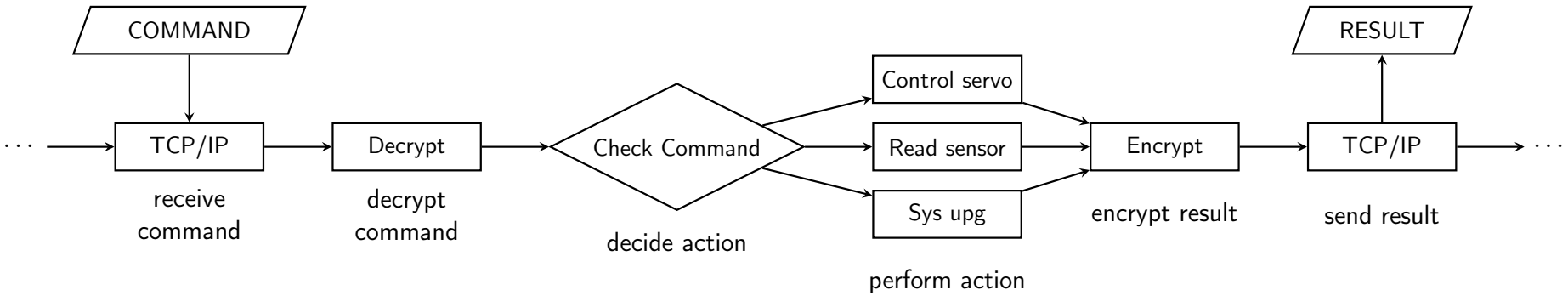

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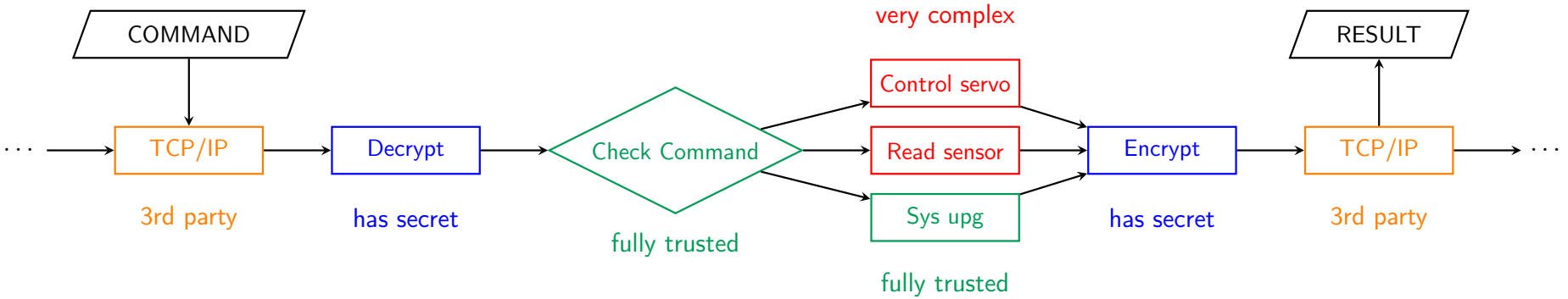
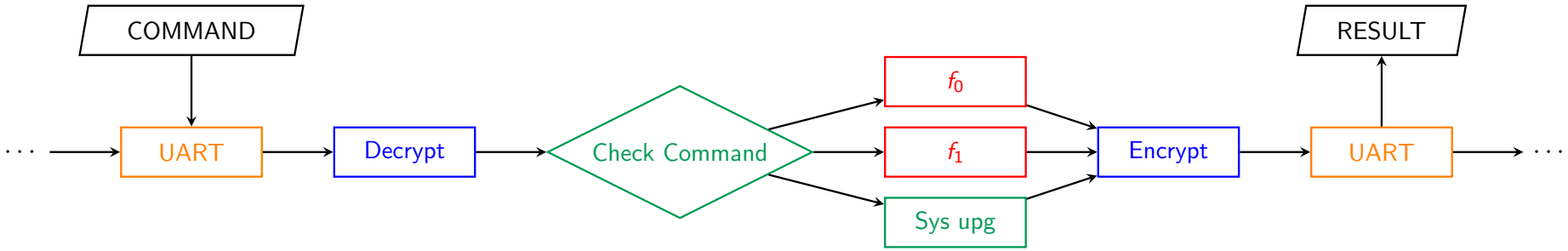


- Monitor – Monitors system & handles commands
- Functions – Interact with environment and output data
- TCP/IP – Handle TCP/IP communication
- Crypto engine – Encrypts & Decrypts Packages

Proof-of-Concept



- Monitor – Manage apps & handles commands
- Dummy Functions f_0, f_1 – Process and output data
- UART – Handle UART communication
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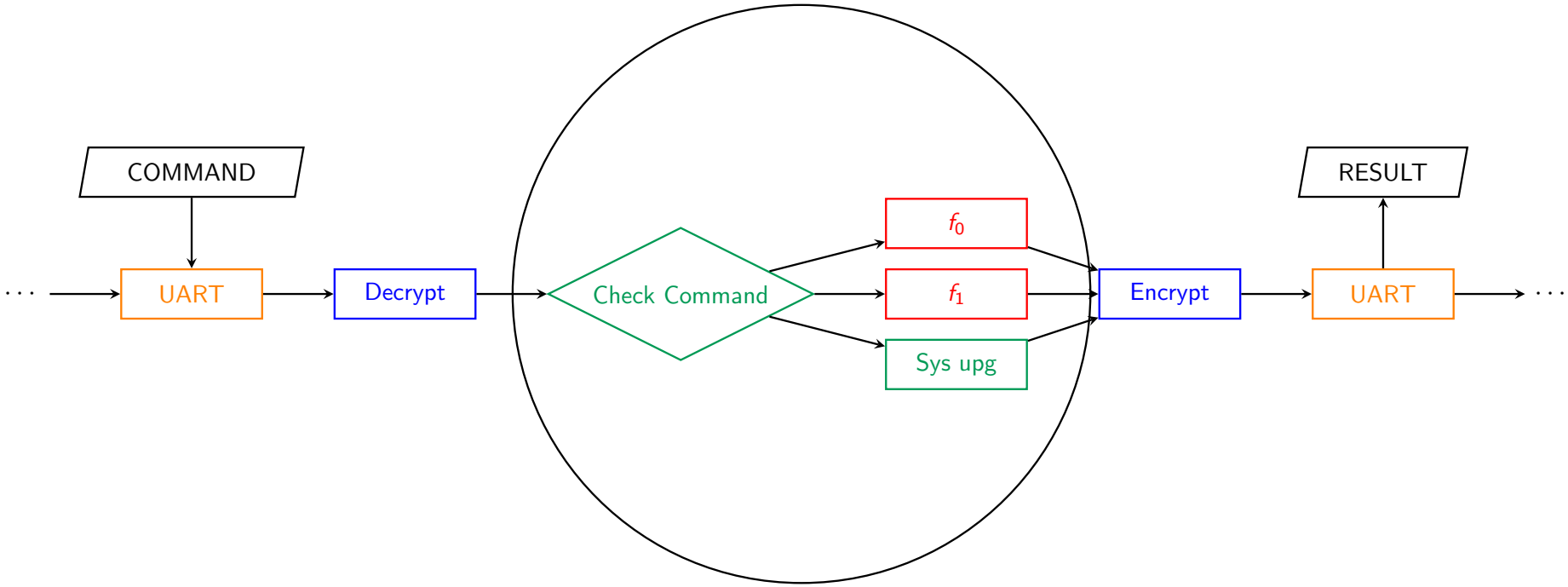

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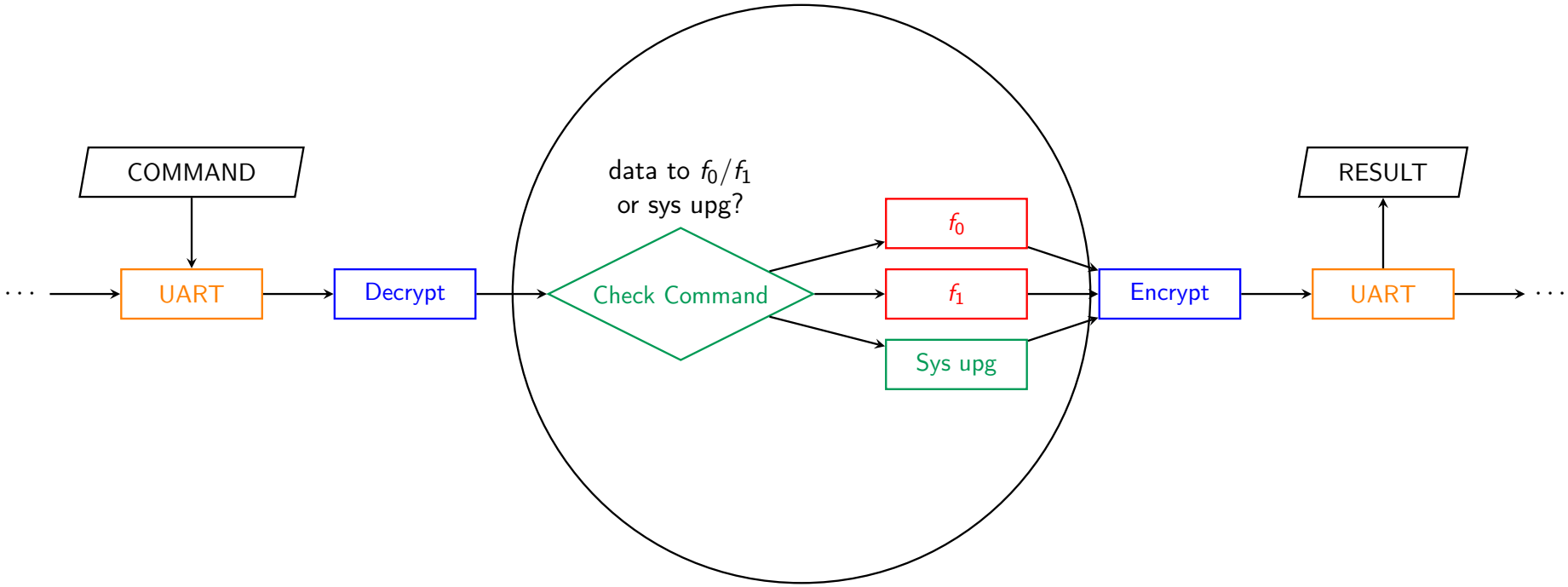

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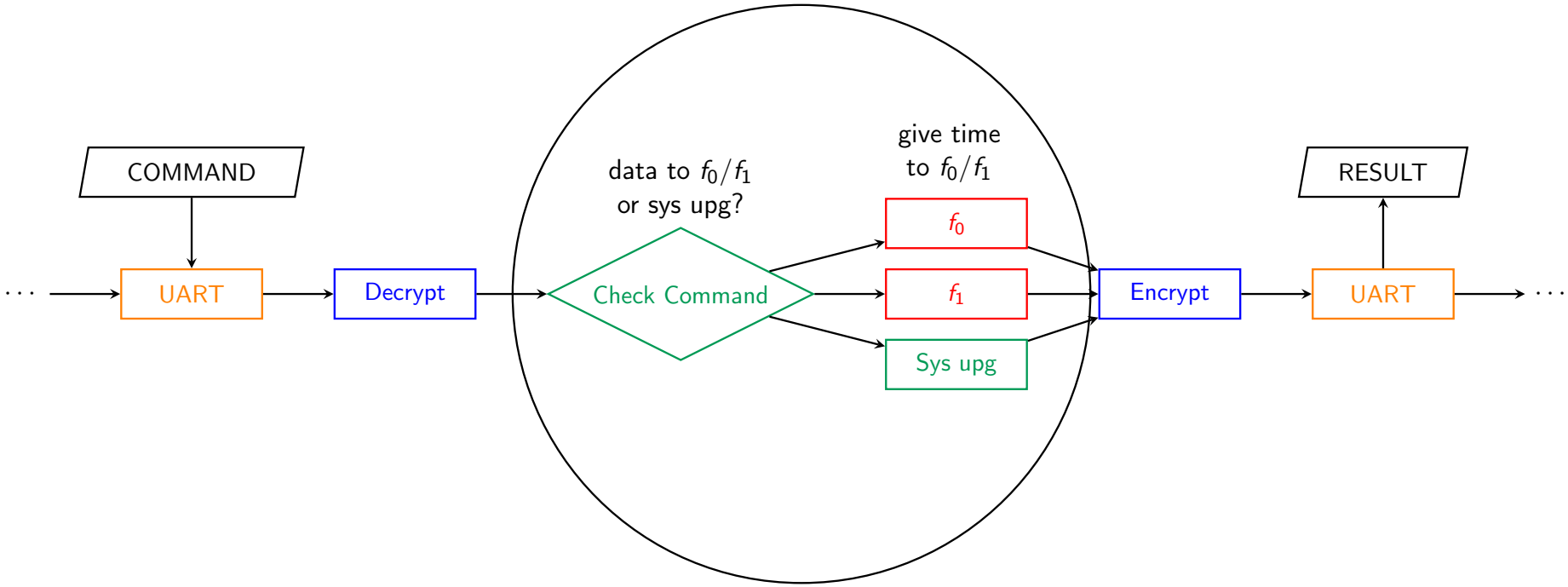

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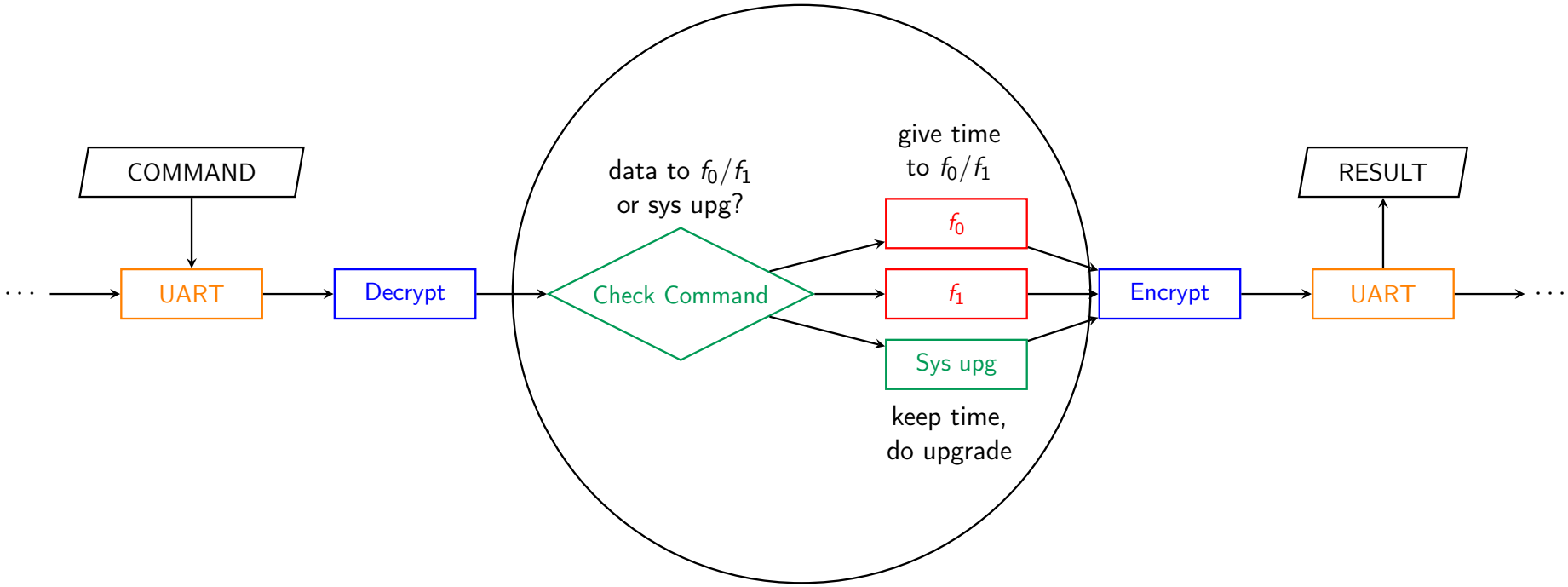

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- $\sim$ 2000 lines of C/Assembly

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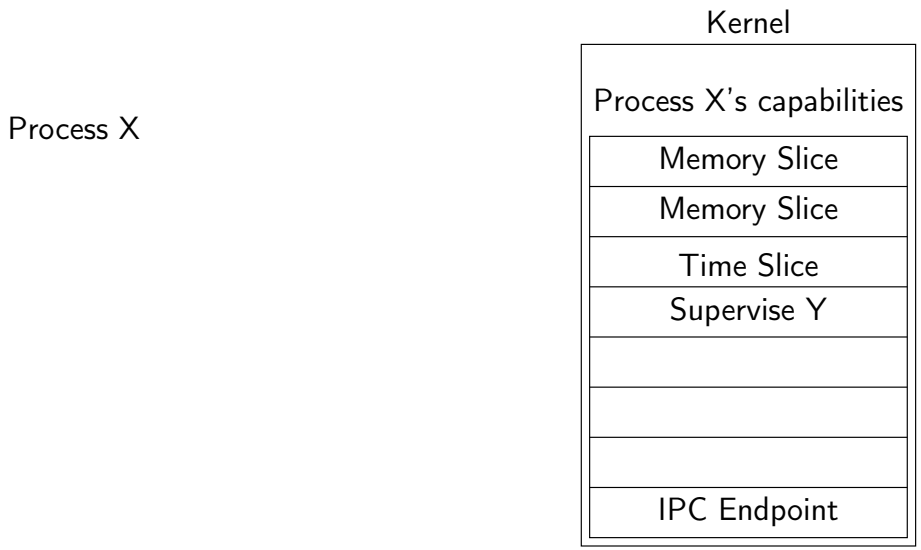
Capabilities

Previously mentioned features are implemented using capabilities

- Capability = object in kernel representing a resource



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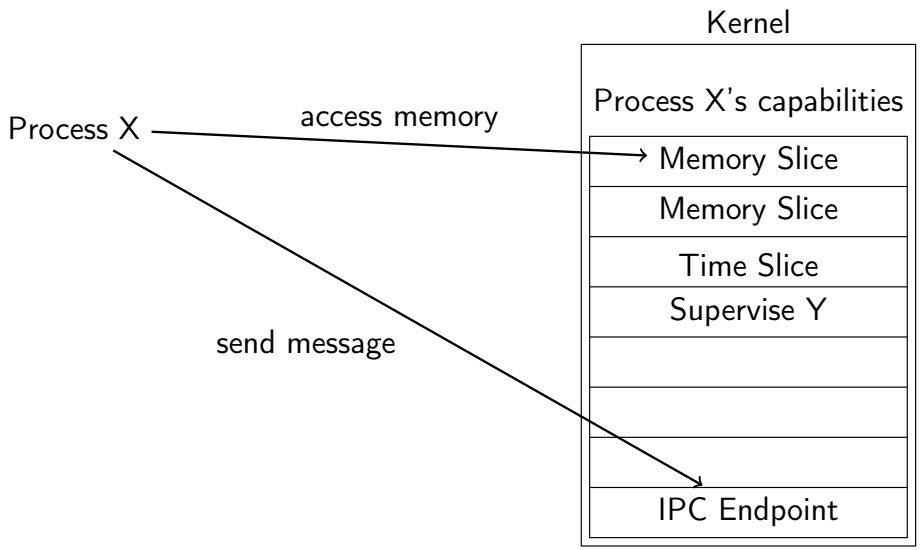

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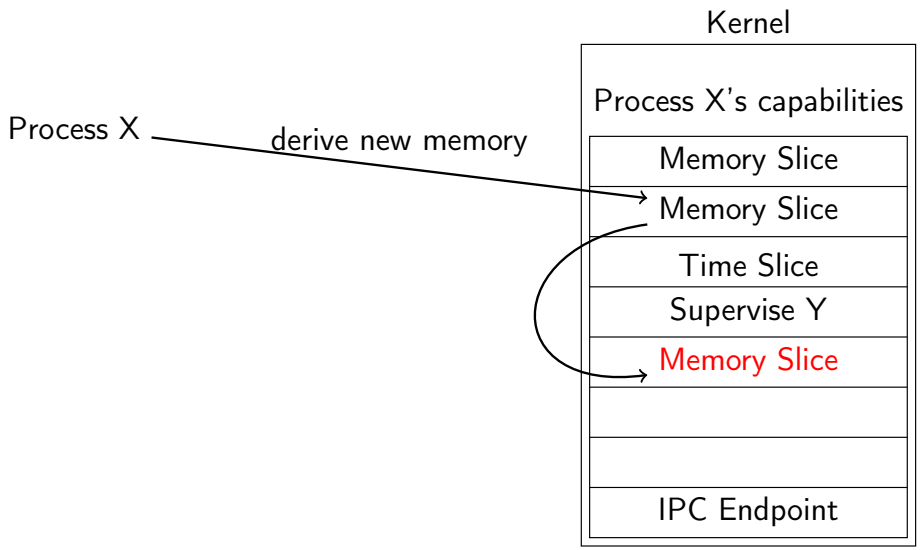

S3K Capabilities

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- Supervisor – Manage a set of processes.

S3K Process Scheduling

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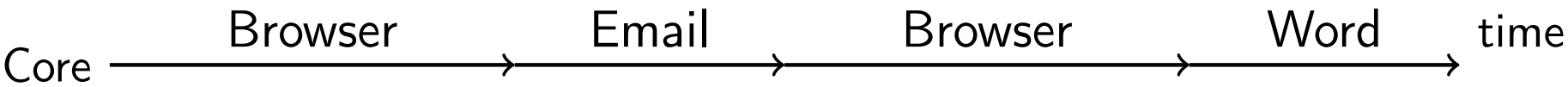

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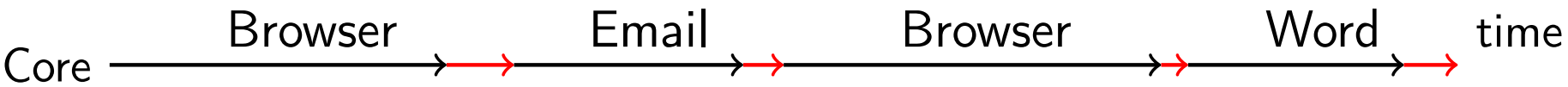

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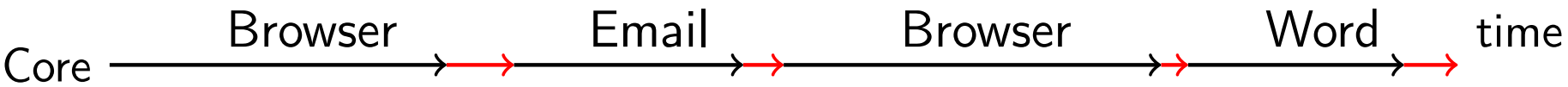

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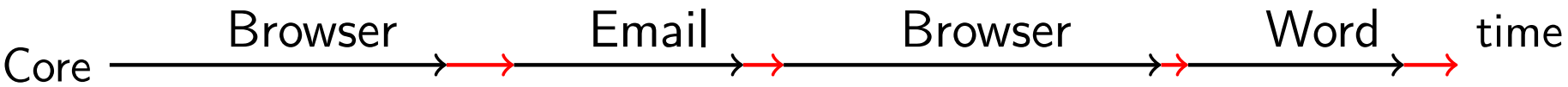

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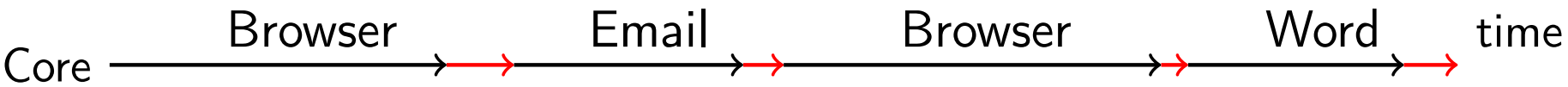

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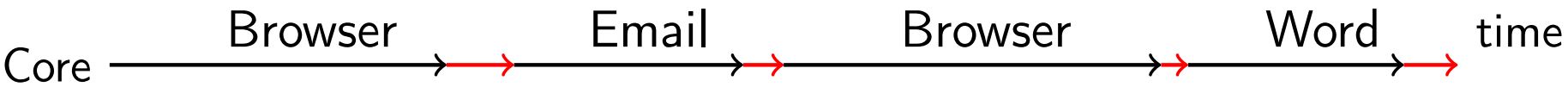

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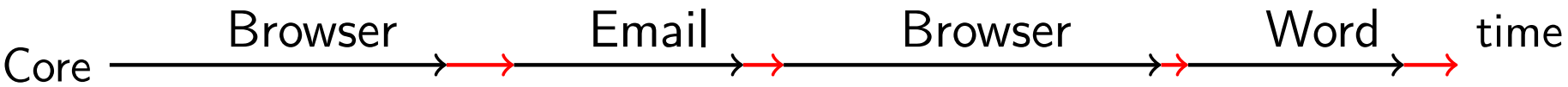

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  - Prevent side-channels attacks? Secure servers, routers, ...

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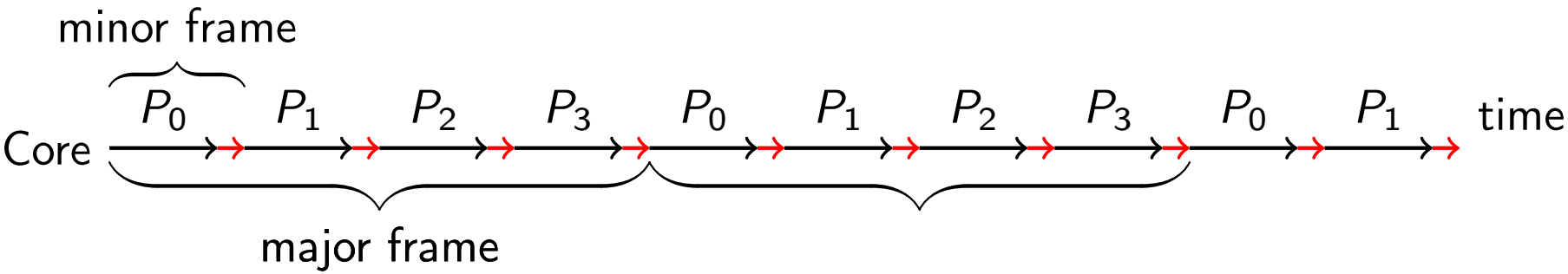
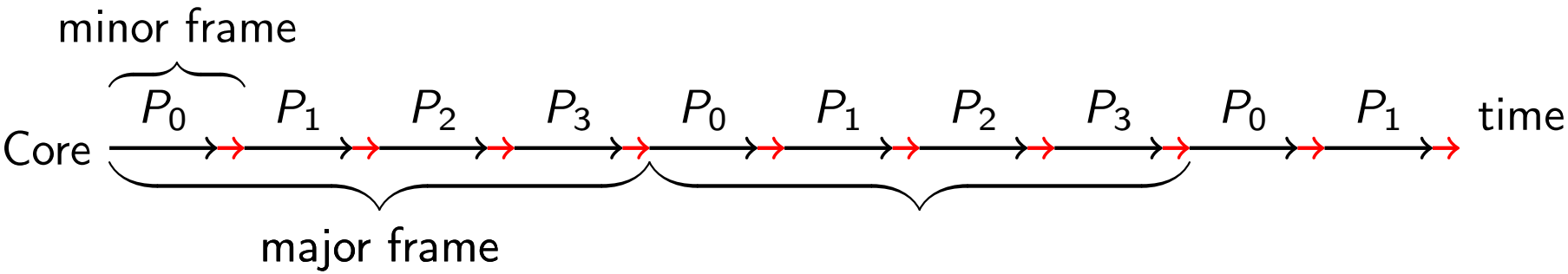


- Modified RR – Minor frames defined by time slice capabilities.

S3K Scheduling



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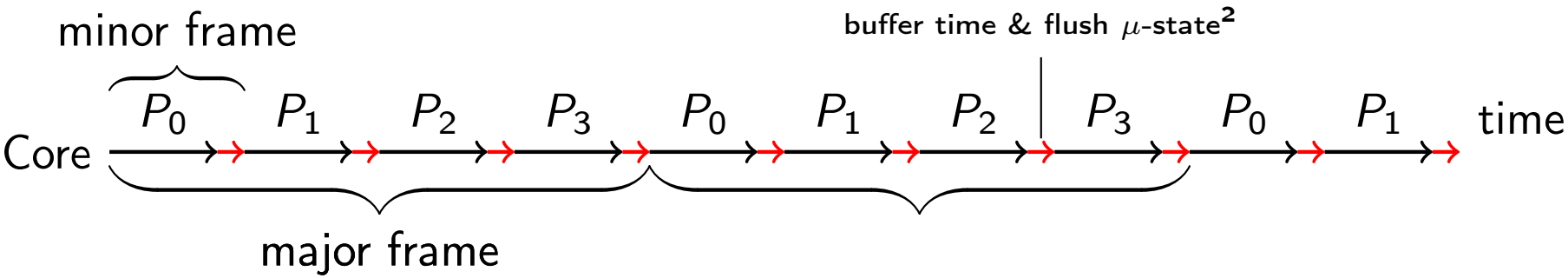

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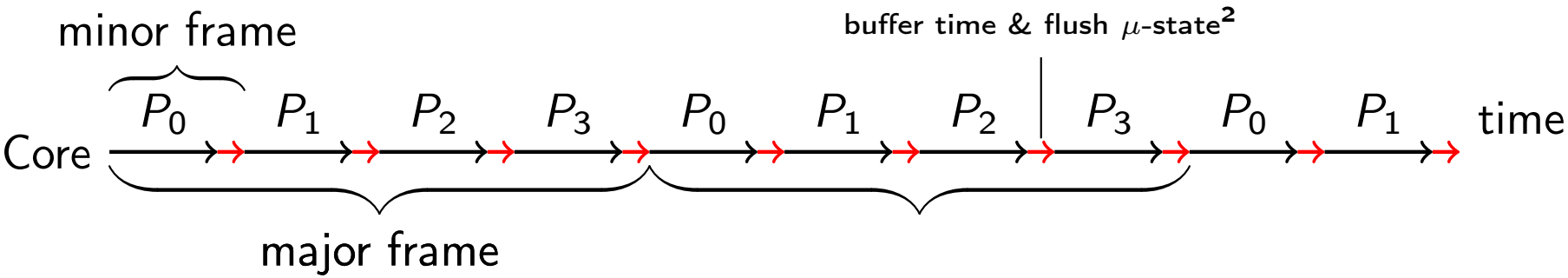
[2] Flush cache, branch predictors, etc., support is hardware dependant.

S3K Scheduling



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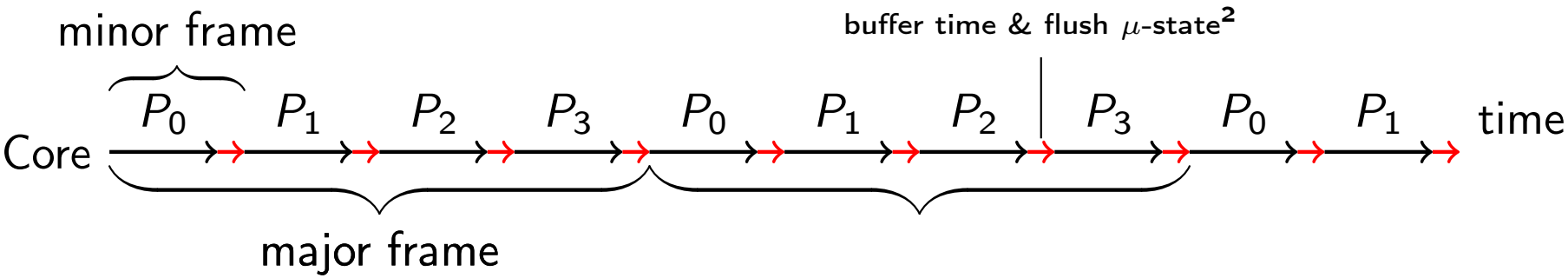

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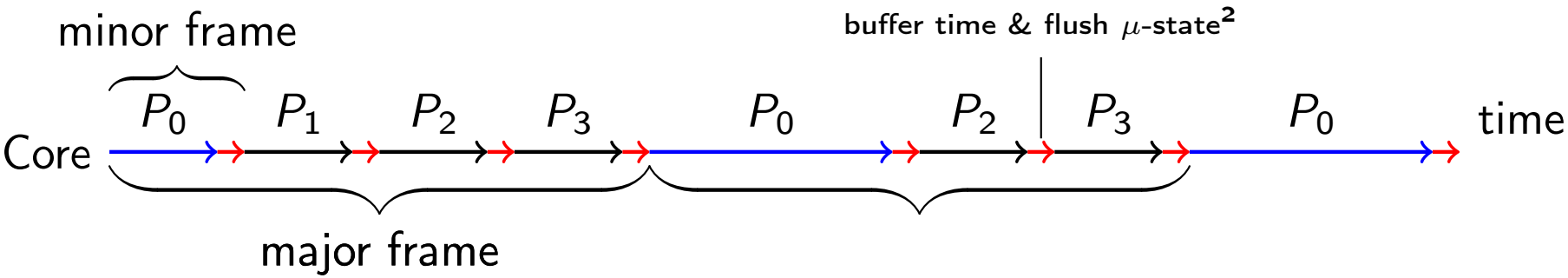

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- Dynamic – Process can alter their time slices.

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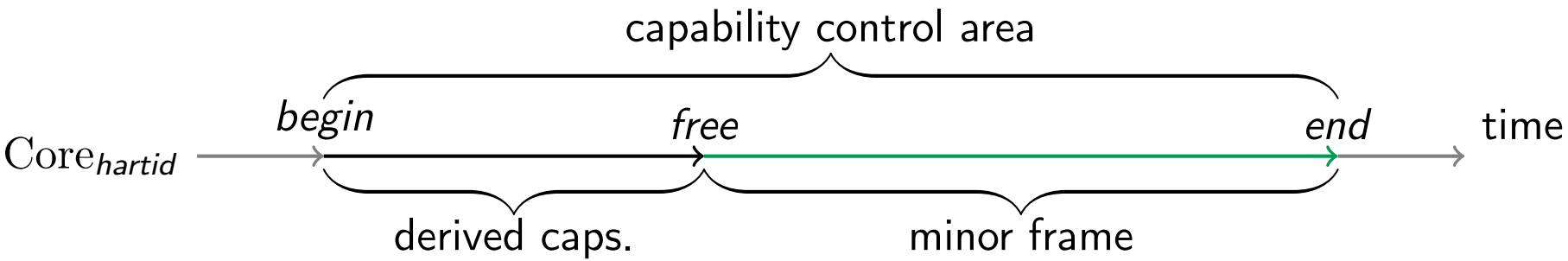
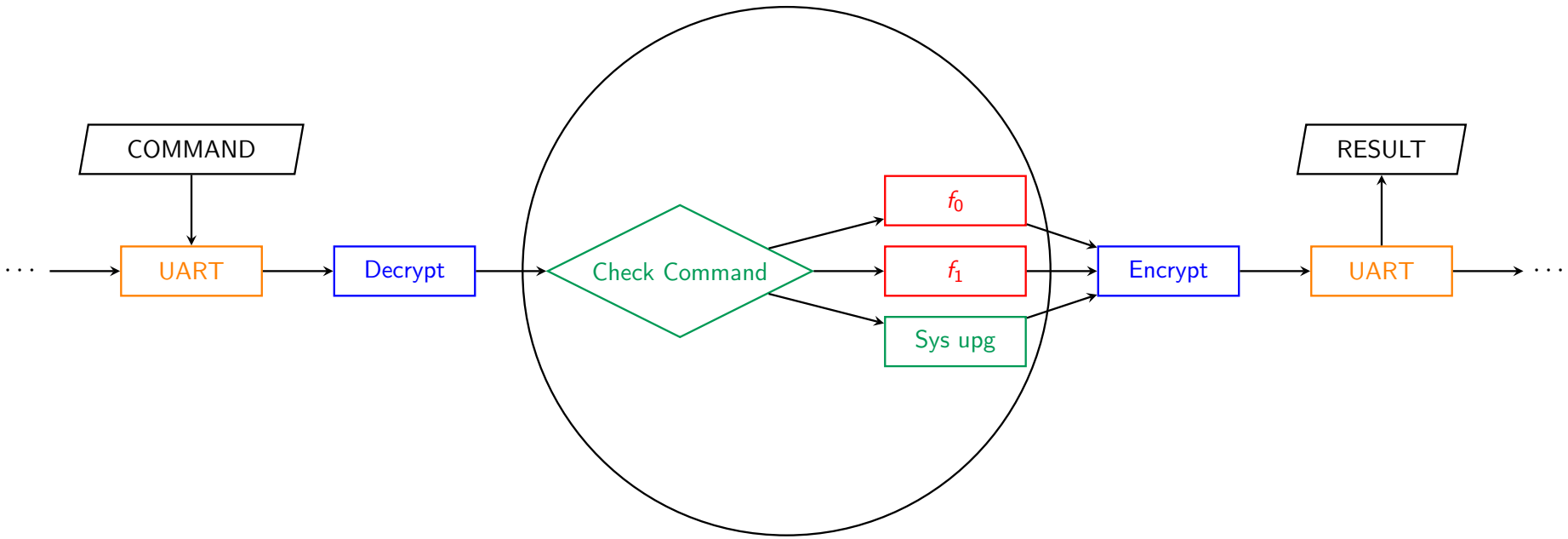
Time Slice Capability



- hartid – ID of a hardware thread.[3]
- begin – start of a time slice
- free – start of minor frame
- end – end of a time slice and minor frame

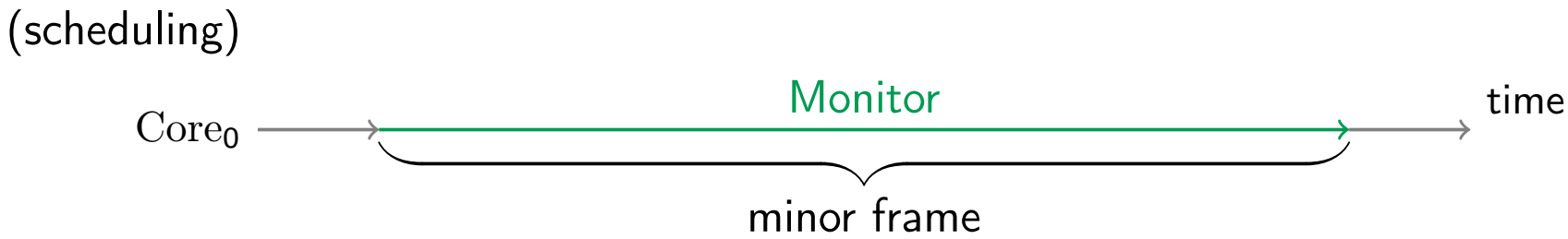
[3] Hardware Thread – Logically separate processor.

Proof-of-Concept with Time Slices



Proof-of-Concept with Time Slice

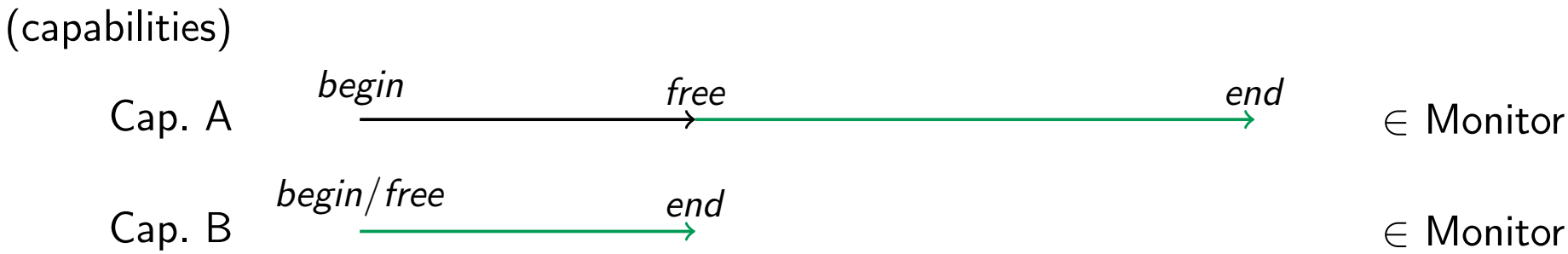
Monitor has the initial time slice

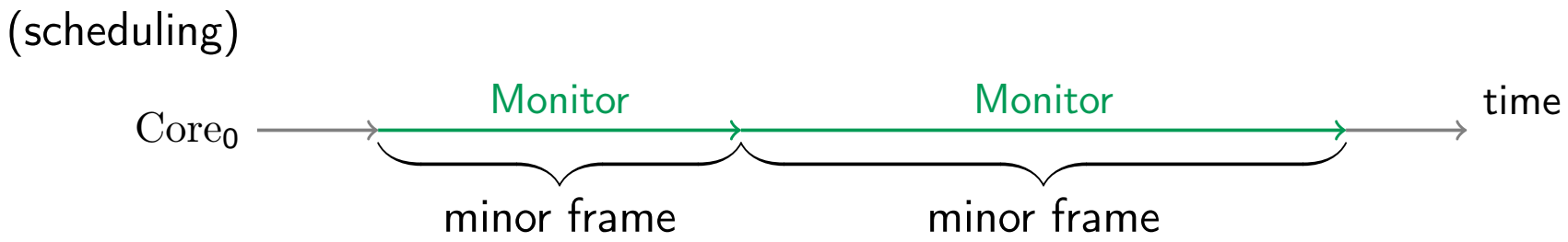


Proof-of-Concept with Time Slice

Monitor derives capability B

(only create slices from *free* to *end*)





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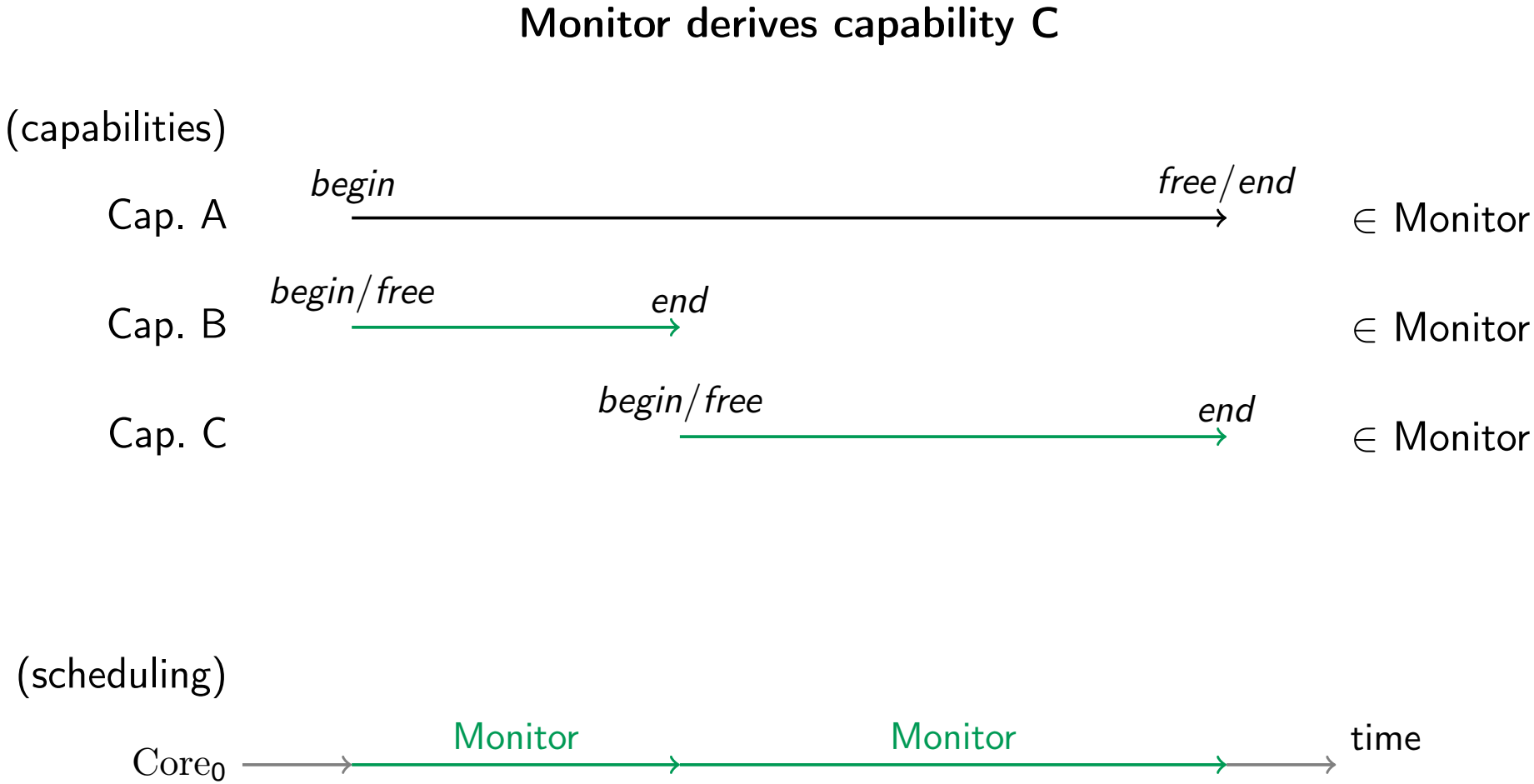

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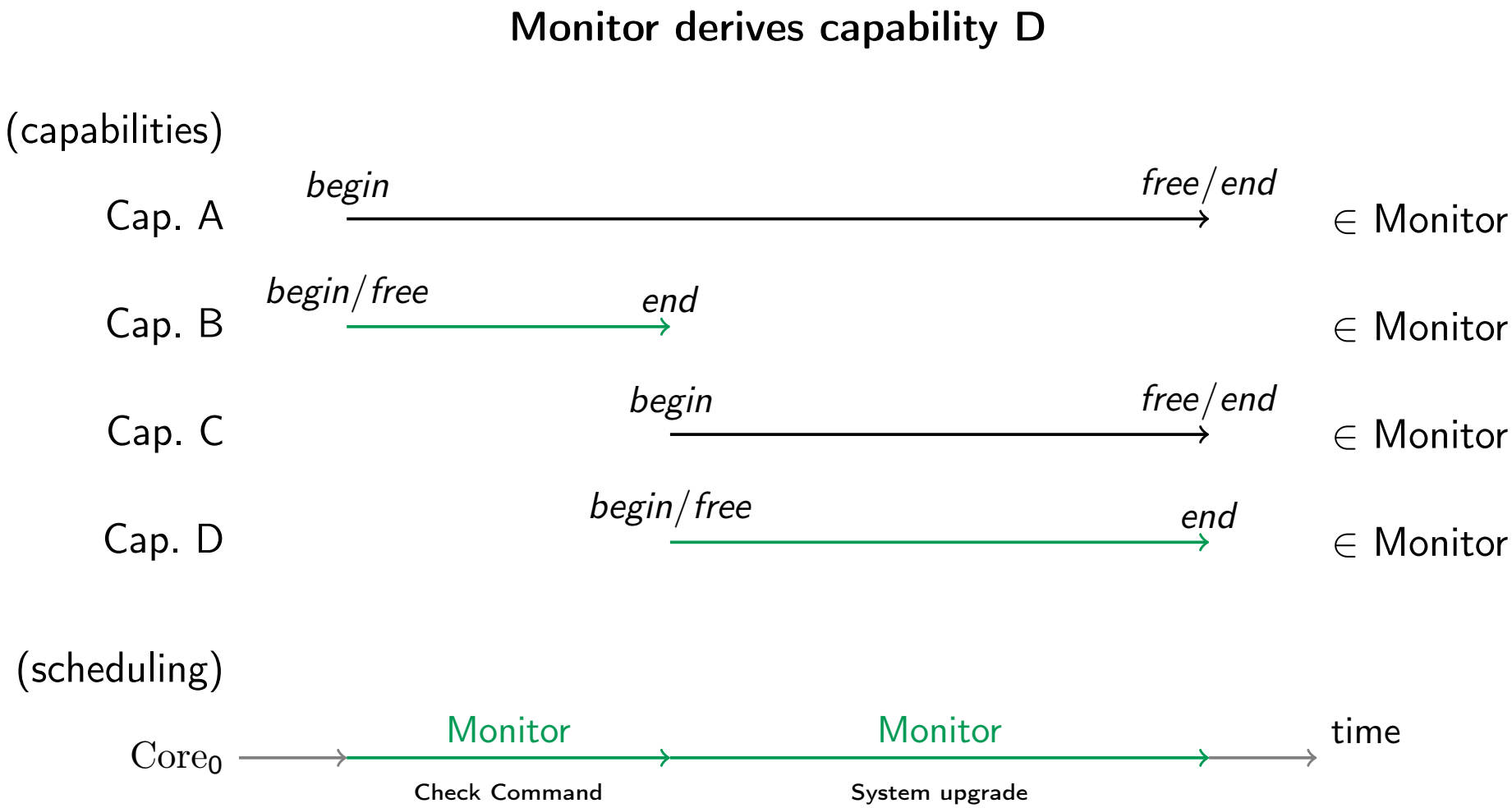

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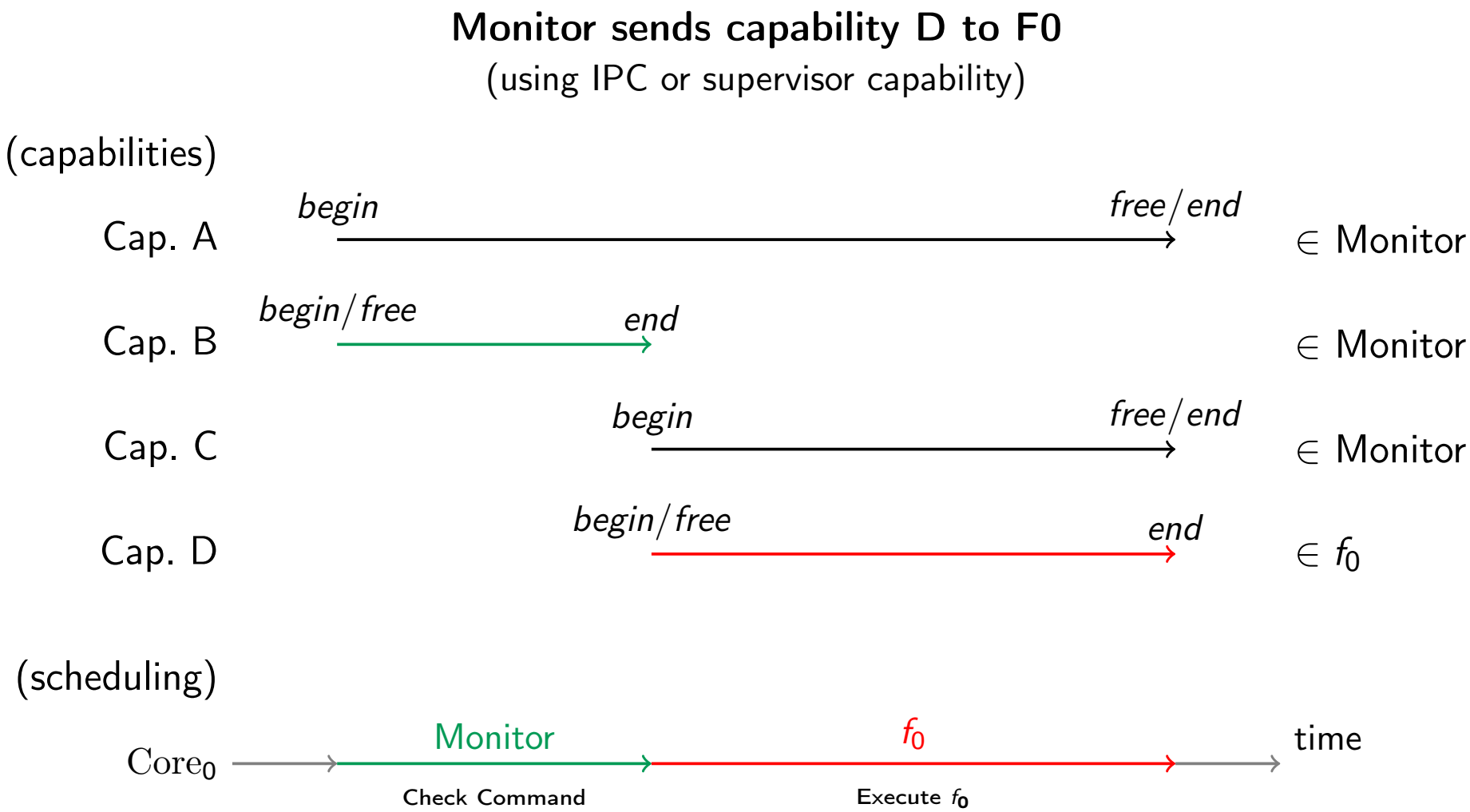

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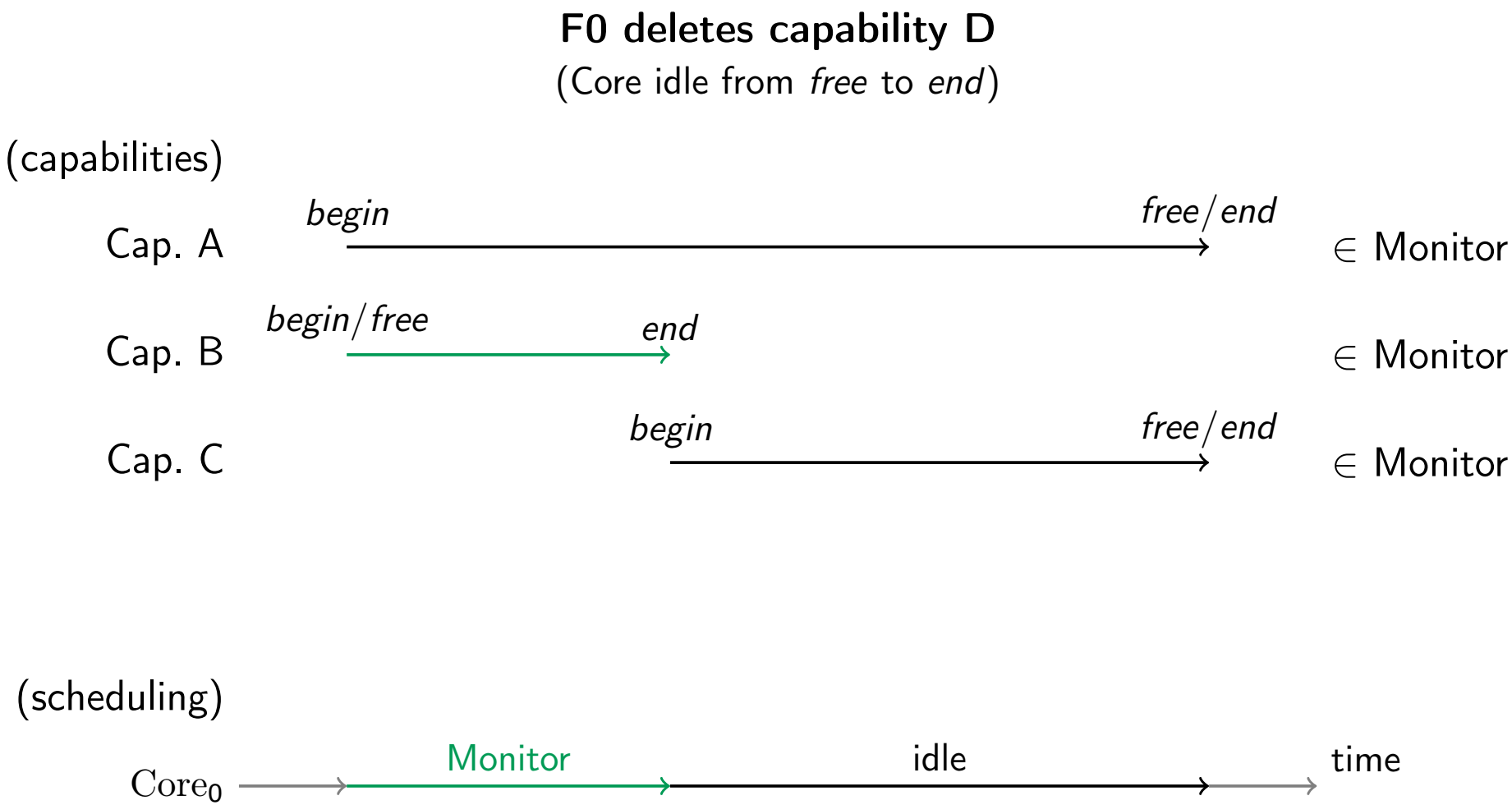

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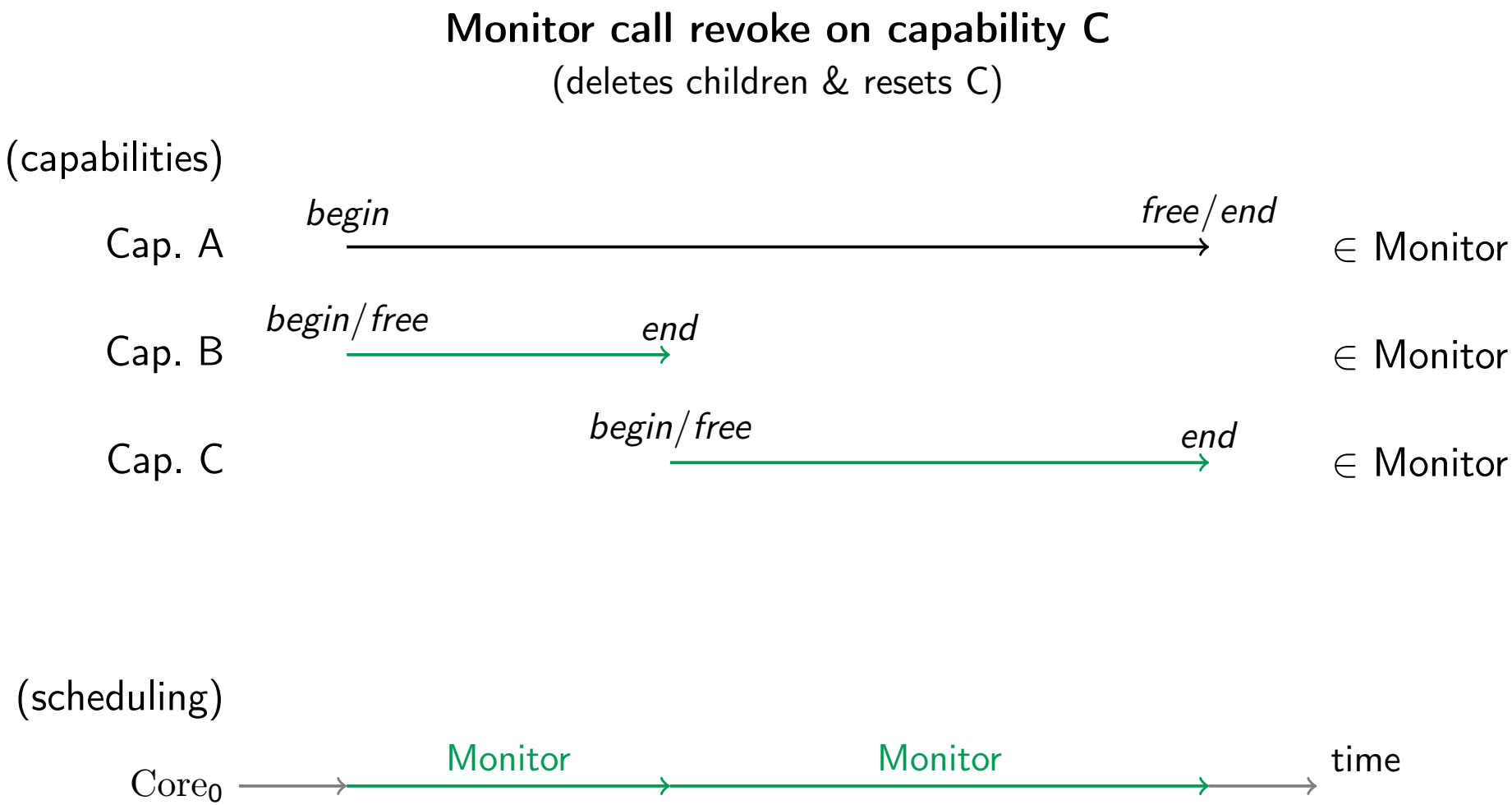

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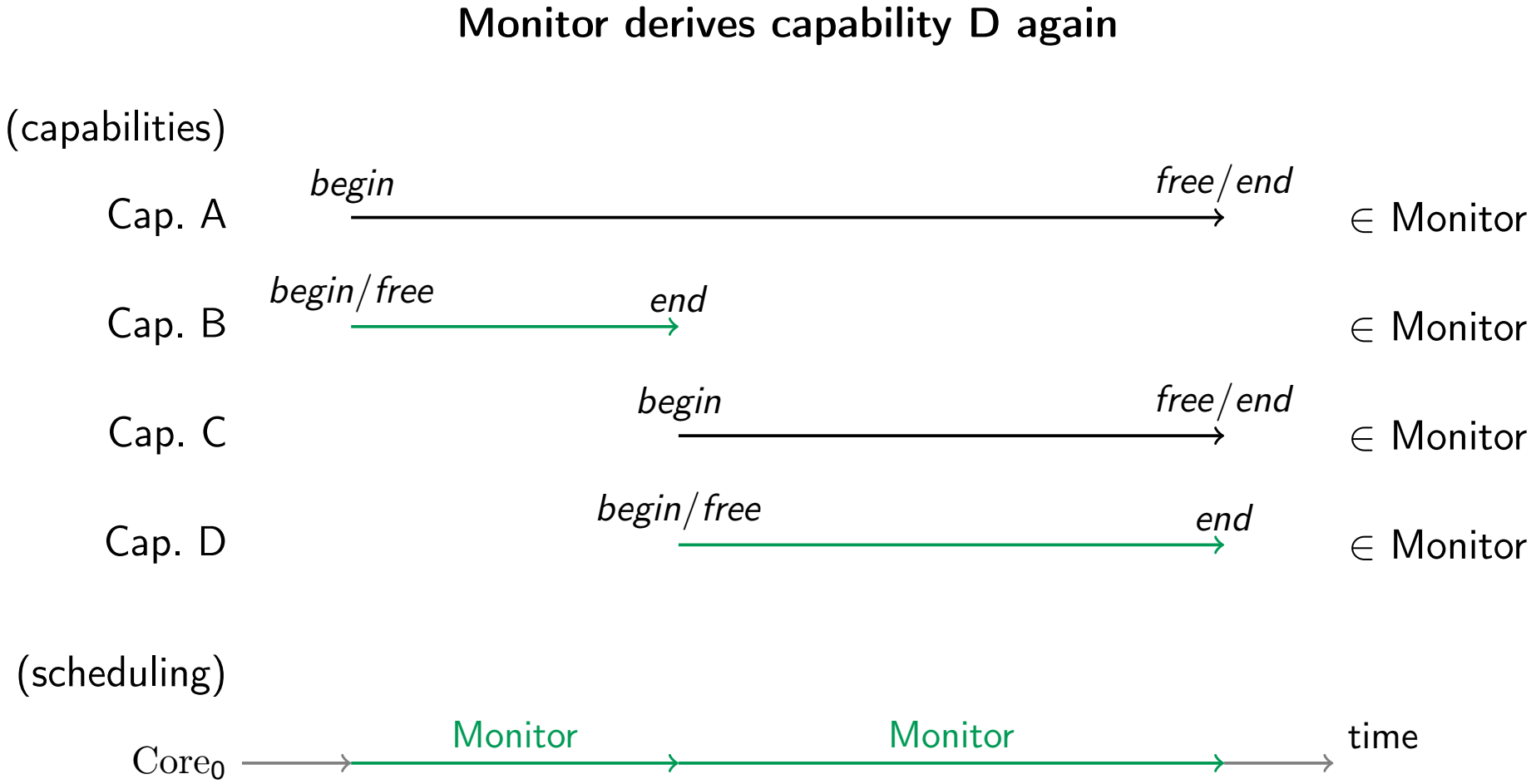
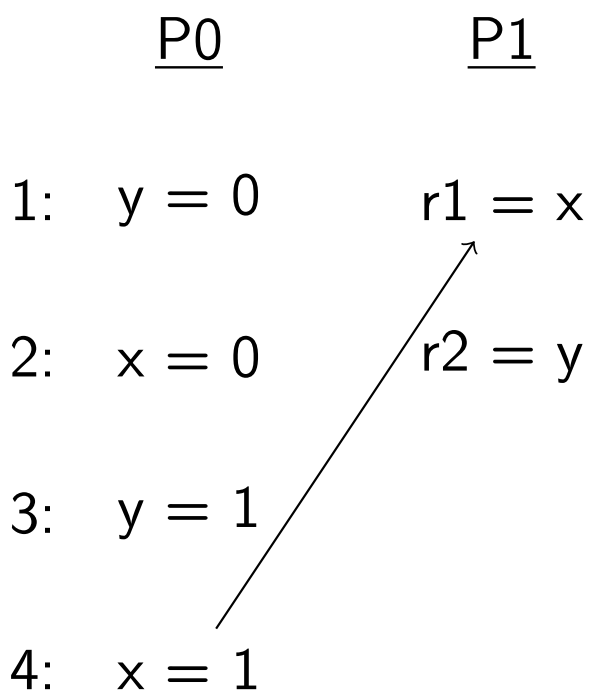


Multicore HolBA & Kernel Verification

Multicore HolBA



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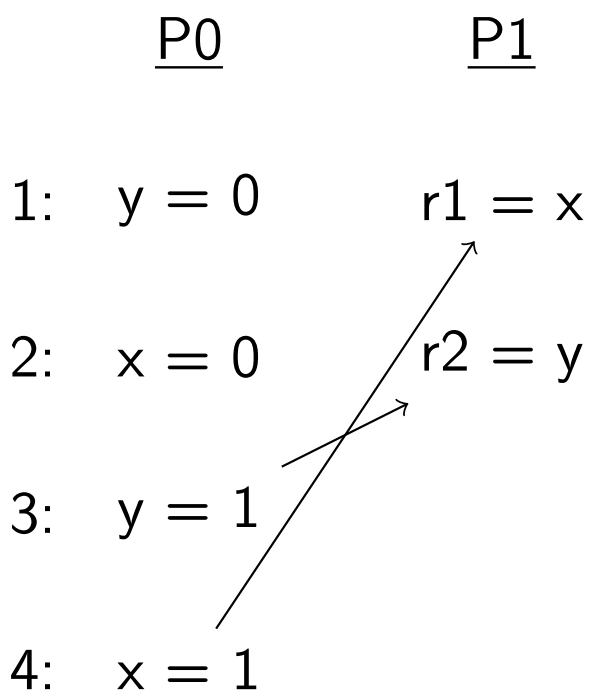

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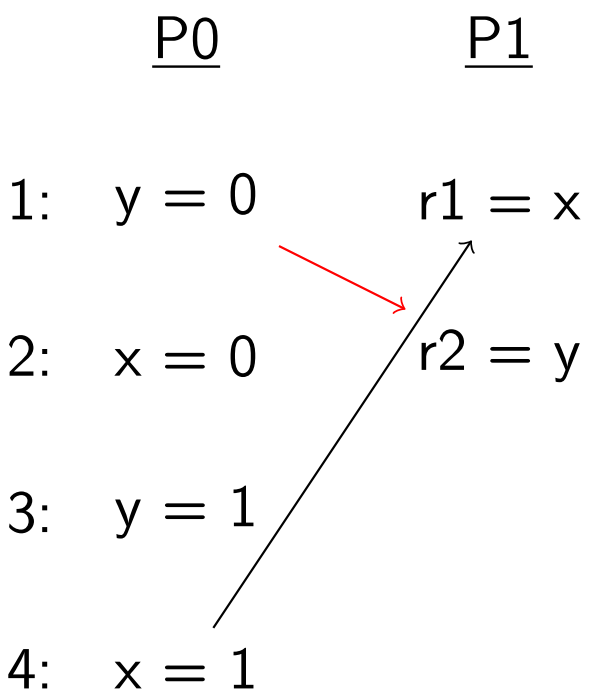
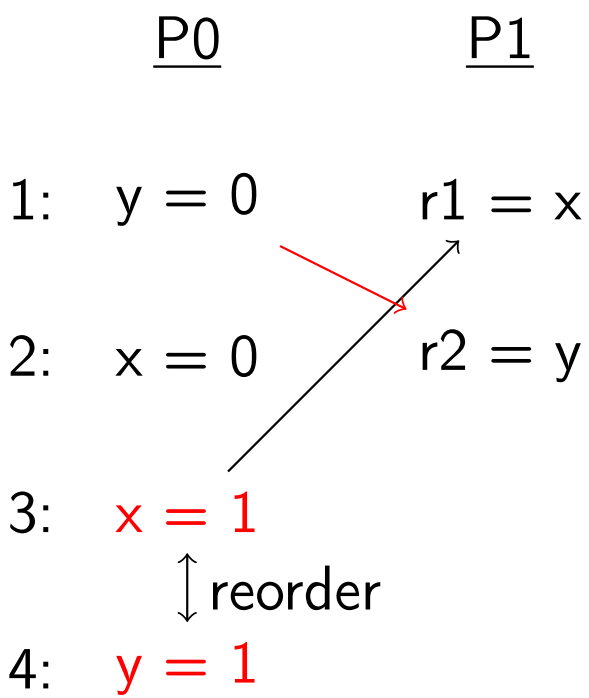


Memory operations may be reordered in RISC-V.

Multicore HolBA



Writes may be reordered.

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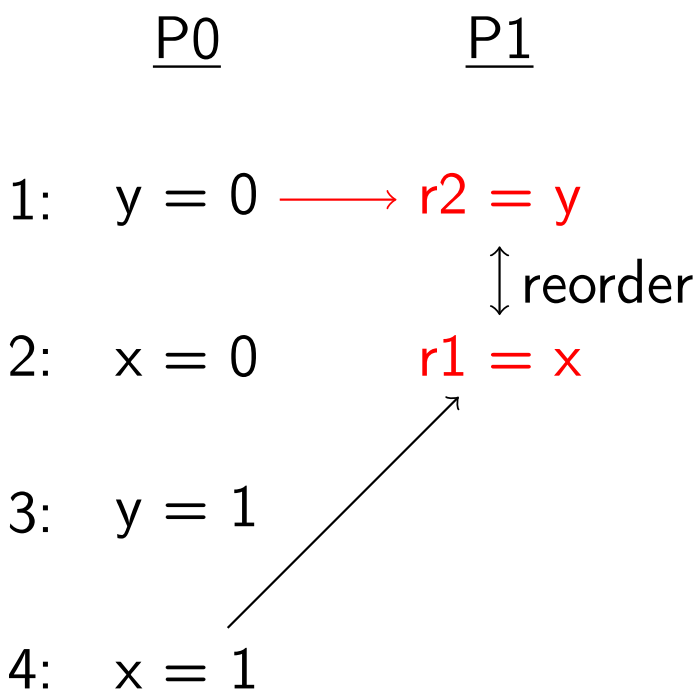

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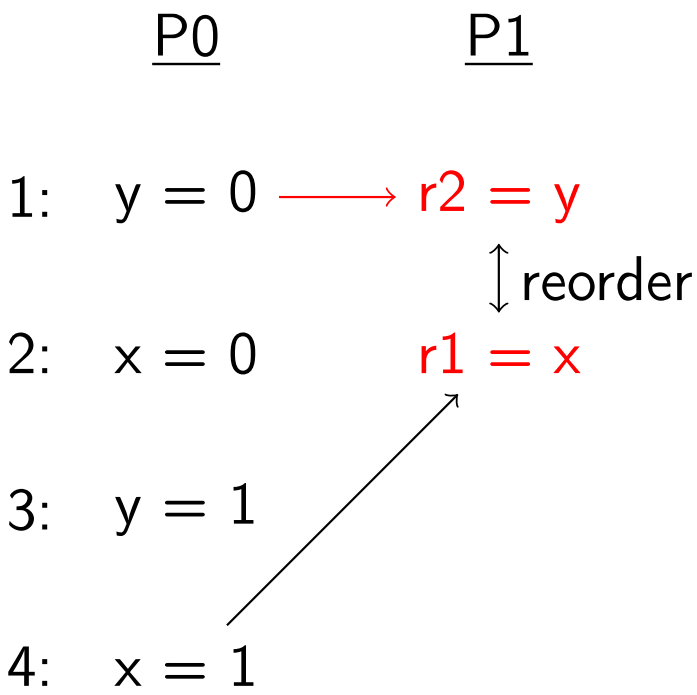
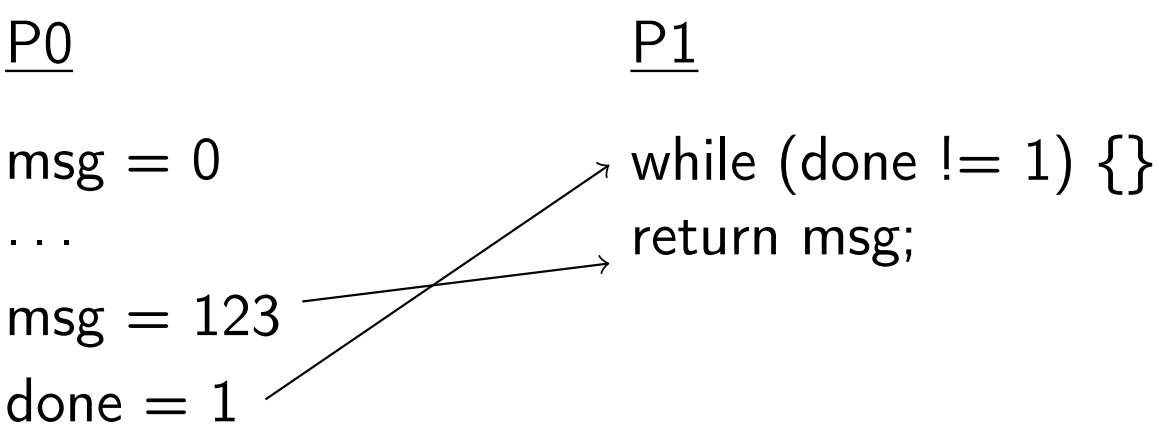


Verification of multicore RISC-V need all reorderings.
Multicore HolBA provides this!

Separation Kernel Example



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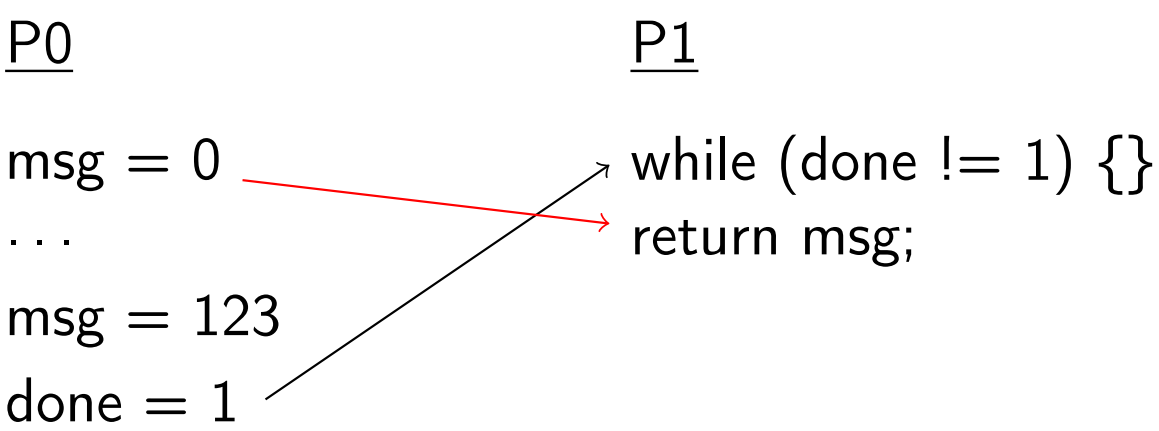

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- Jan./Feb. 2023 – Evaluation and publication of kernel with proof-of-concept

[4] Worst-case execution time

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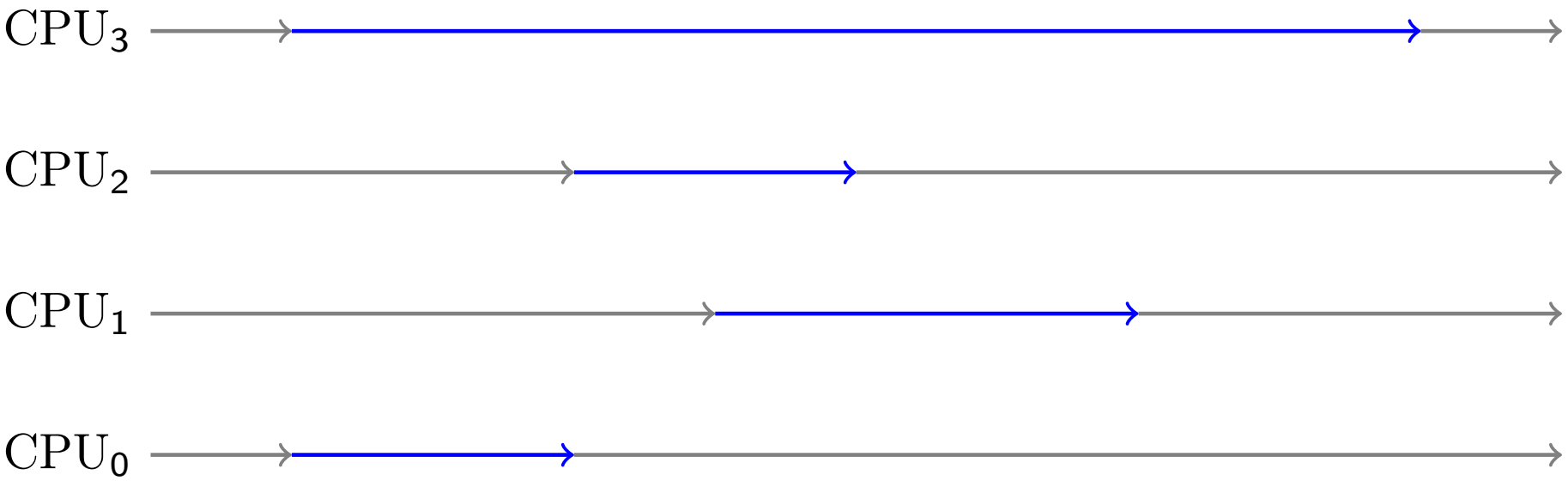
[4] Worst-case execution time

Questions?

Multicore Scheduling

Where does the blue process execute?



Process runs on one core, for determinism,[5] we need priority rules.

- currently running core
- core with smallest ID.

[5] non-determinism may leak information

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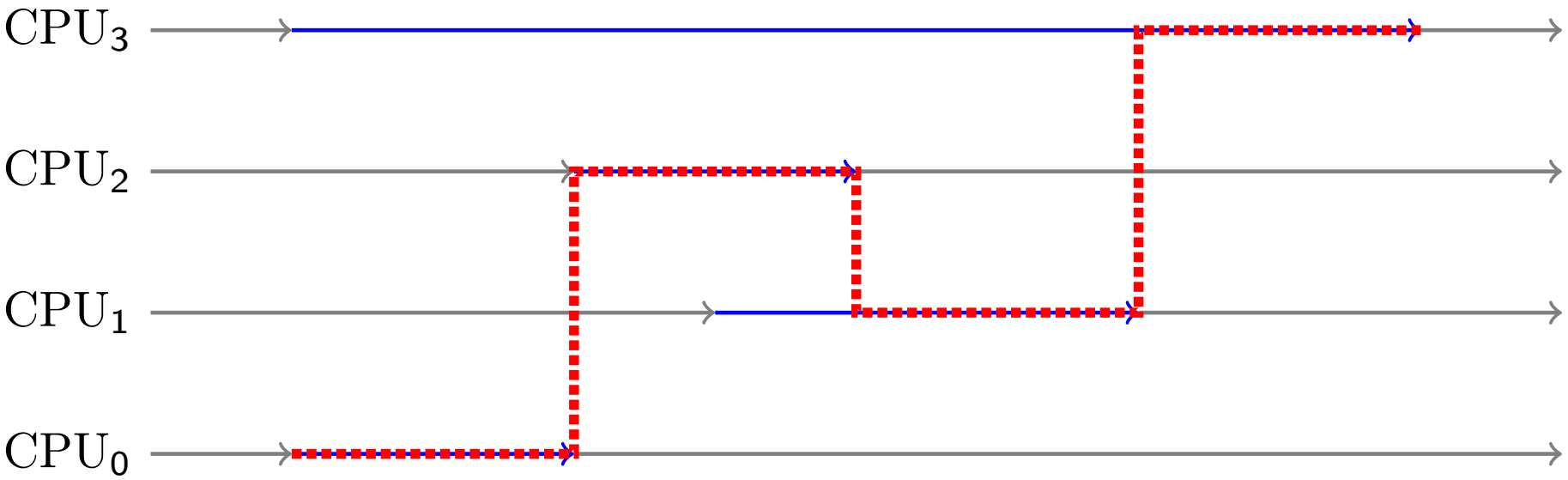

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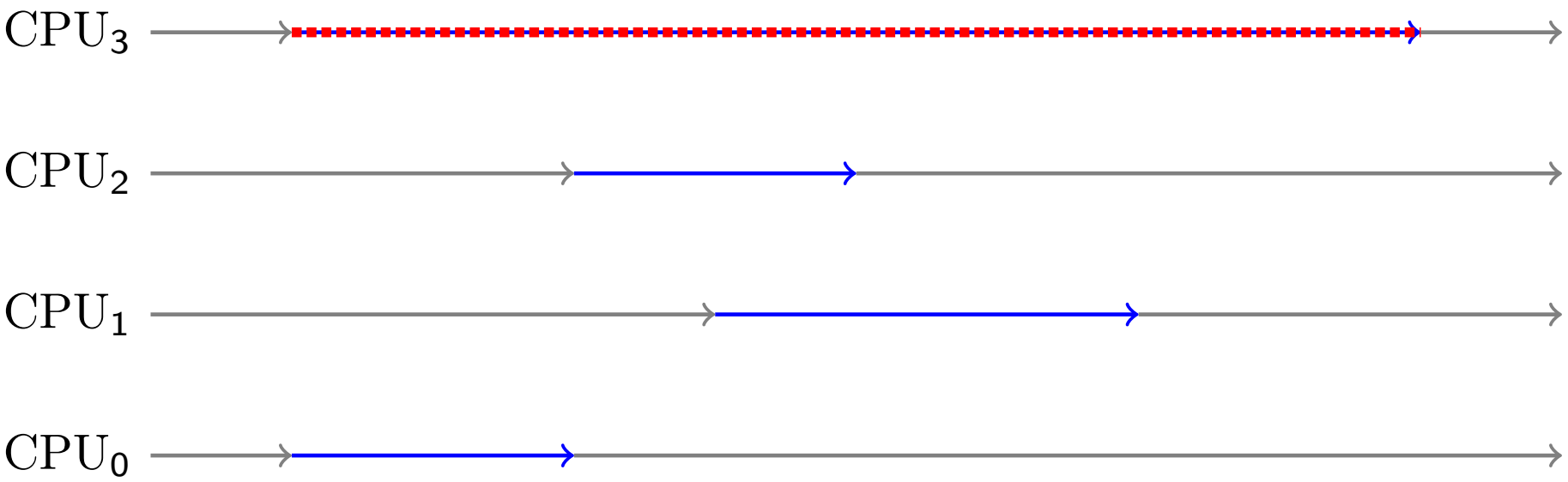

Process runs on one core, for determinism,[5] we need priority rules.

- currently running core
- longest quantum (not implemented)
- core with smallest ID

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